Analysis of the electrical behavior of silicon rich silicon oxides

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ABSTRACT:

The electrical behavior (capacitance–voltage and current–voltage) of MOS-like structures with silicon rich silicon oxide (SRO) as the dielectric material has been studied. The SRO active layer has been obtained by three different CMOS compatible techniques, namely low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD) and ion implantation. Different silicon excesses have been analyzed. The results have been related to the electroluminescent behavior of the samples. Two different conduction regimes have been identified: a high leakage regime and a low leakage regime. The former is related to an anomalous C–V behavior and to the luminescence from a limited number of dots in the area of the devices whereas the latter is related to a regular C–V behavior and to the homogeneous luminescence of the whole area of the devices.

Key words: LPCVD, PECVD, implantation, silicon, nanoparticles, electroluminescence

1 Introduction

Despite the huge success of silicon in the electronics industry, it falls short of the efficient optical emission shown by direct band gap semiconductors. Since Canham first demonstrated light emission from silicon nanostructures back in 1990[1], a lot of effort has been devoted to overcome the inherent limitations of bulk silicon as a light emitter.

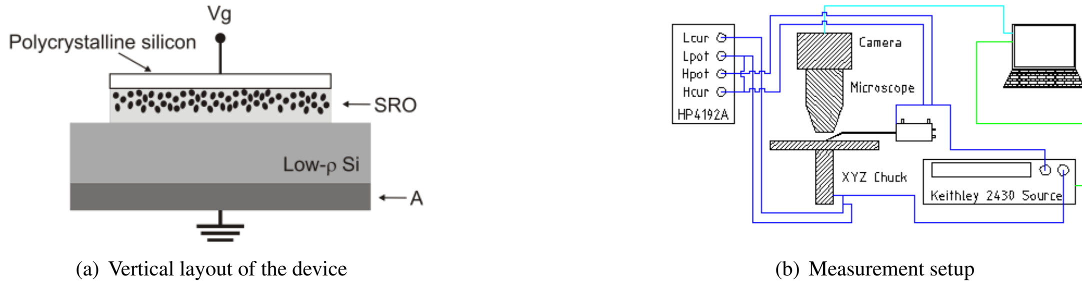
In the last years, materials based on silicon nanoparticles embedded in silicon dioxide[2, 3, 4, 5, 6, 7] and silicon nitride[8, 9, 10, 11] have been shown to be good light emitters, though still far from the efficiencies of conventional LEDs.

Silicon nanoparticles embedded in a dielectric matrix can be fabricated by a number of techniques. Particularly interesting are low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD) and ion implantation, for these technologies are CMOS compatible and therefore make possible the monolithic integration of a silicon based light source in a conventional electronic circuit. These techniques allow us to obtain materials with similar electro-optical characteristics but with diverse electrical behaviors.

In order to analyze the effect that the fabrication technique has on the electrical behavior of the SRO materials, in the following sections we present the C–V and I–V characteristics of electroluminescent metal-oxide-semiconductor (MOS) structures with silicon nanoparticles embedded in the dielectric layer[12], fabricated by LPCVD, PECVD and ion implantation. These are preliminary results of an in depth study of the mechanisms responsible for the electroluminescence in SRO materials.

2 Experimental

We have fabricated MOS structures as depicted in figure 1, where the active layer is formed by silicon rich silicon oxide instead of regular silicon dioxide. The



(a) Vertical layout of the device

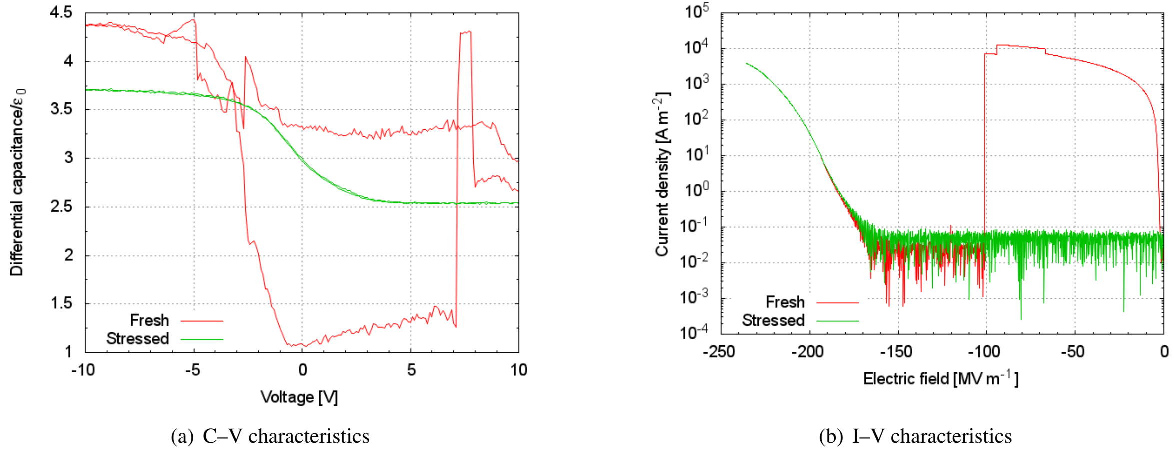
(b) Measurement setup

Figure 1: Vertical layout of the device and measurement setup

active layer is grown/deposited on a 0.1–1.4 Ω·cm silicon substrate. Three sets of samples will be studied here, each with its active layer fabricated by one of the previously mentioned CMOS compatible techniques, namely LPCVD, PECVD and ion implantation.
The LPCVD and PECVD SRO layers were obtained adjusting the ratio between the precursor gases ($[SiH_4]/[N_2O]$). Samples with different ratios have been fabricated, thus leading to different silicon excesses in the active layers. More details on the preparation of the SRO samples have been published for LPCVD[13] and PECVD[7].
For the implanted samples, a 40 nm thick thermal silicon oxide is grown on the silicon substrate, followed by the deposit of a 30 nm thick silicon nitride layer used to control the silicon implantation process, which was removed after the annealing process.
Two silicon ion implantations were carried out[14] in each sample with varying doses (between $1.2 \cdot 10^{16}$ and $8.3 \cdot 10^{16}$ cm^{-2}): the first one at 25 KeV and the second one at 50 KeV. The implanted dose during the 50 keV process is four times the implanted dose during the 25 keV implantation. This ratio between the 25 and 50 keV implantations leads to a rather homogeneous distribution of the implanted silicon ions across the silicon oxide layer according to SRIM[15] simulations.
The experimentally obtained silicon excesses and thicknesses of all the samples can be found in table 1
Once an SRO layer is obtained, a thermal annealing is carried out to induce the formation of silicon nanoparticles in the dielectric layer[7, 13, 14]. The selection of annealing temperatures and durations have been based on previous results[7, 13, 14] and are referenced in table 1. In the case of the ion implanted samples, the silicon nitride layer used during the implantation process is removed after the annealing.
The device fabrication continues with the deposition and doping process of a 350 nm n–type polysilicon layer followed by photolitography and etching to define the transversal layout of the gate (squares of sides 500 μm). Next, an aluminum layer of 1000 nm is deposited followed by a second photolitography step and etching process to define the contact pads. Finally, the back contact is formed by sputtering of an aluminum layer followed by an annealing process.
The electrical measurements were performed in a Karl Süss probe station, with Süss Microtech PH120 probeheads and 7 μm tungsten probes.
Current-voltage characteristics were obtained with a Keithley 2430 source-meter and capacitance-voltage

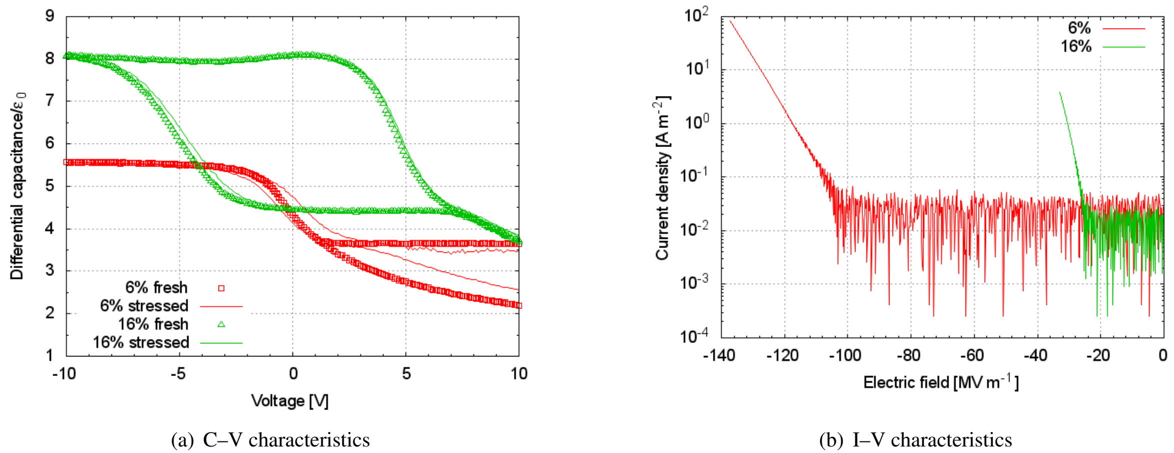
Technique	Si. exc [%]	Thickness [nm]	Ann. temp. [°C]	Ann. duration [min]
LPCVD	6	53 ± 3	1100	180
	7	35 ± 5		
	19	20 ± 3		
PECVD	6	53 ± 5	1250	60
	8	55 ± 6		
	12	60 ± 9		
	16	59 ± 7		
Ion Implantation	12	40 ± 5	1100	240
	13	43 ± 4		
	14	44 ± 9		
	15	44 ± 4		
	17	22 ± 1		

Table 1: Sample characteristics according to the fabrication technique



(a) C–V characteristics (b) I–V characteristics

Figure 2: Electrical characteristics obtained in LPCVD samples with 6% silicon excess



(a) C–V characteristics (b) I–V characteristics

Figure 3: Electrical behavior of PECVD samples with 6% and 16% silicon excess

characteristics were measured with an HP 4192A LF impedance analyzer.

The measurement protocol has been the same in all samples: firstly, capacitance-voltage characteristic is measured on as-obtained devices (those that have never been electrically stressed previously in any way). Secondly, current-voltage characteristics are measured. Finally the C–V is again measured after the I-V stress.

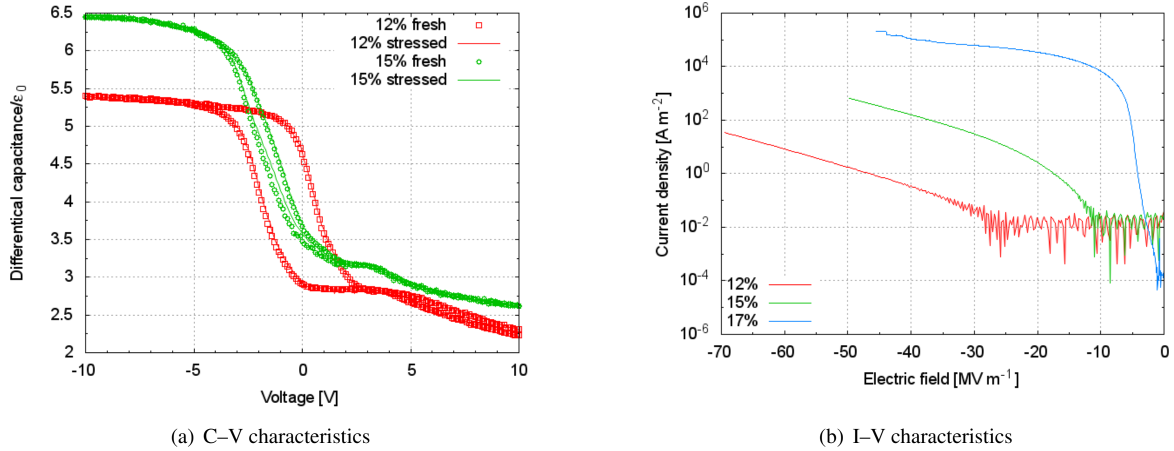
Capacitance–voltage curves have been taken from inversion to accumulation and back to inversion with a voltage ramp of 0.1 V/s and the AC component of the ramp at 100 KHz.

3 Results

Figures 2 to 5 show typical C–V and I–V behaviors of samples with different silicon excess and fabricated using different techniques. For clarity, only the most representative samples have been plotted. In order to eliminate the dependence of the capacitance on the area and thickness of the device, the values have been multiplied by the thickness of the device and divided by its area and the permittivity of vacuum. Therefore, the values of the y–axis of the C–V curves are adimensional and the saturation value in accumulation (negative voltages) tends to the relative permittivity of the medium.

The samples fabricated by LPCVD show two different behaviors: on as-obtained devices the C–V curve is quite anomalous (red line, figure 2(a)). This corresponds to the high leakage current shown in figure 2(b) (red line). In this state, electroluminescence can be seen as bright spots on the surface of the device.

At some point during the electrical stress, the current drops to a low leakage situation[16]. At the same time the luminescent dots disappear[17]. Once in low leakage, the device remains in that state (see green line in figure 2(b), a second I–V measurement). Moreover, if



(a) C–V characteristics

(b) I–V characteristics

Figure 4: Electrical characteristics of implanted samples with 12% and 15% silicon excess

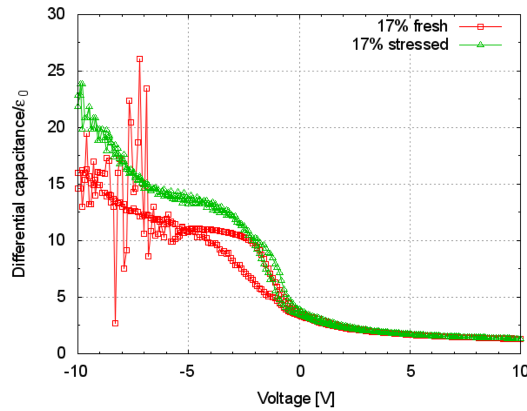


Figure 5: Anomalous C–V curve of the implanted sample with 17% silicon excess

we measure capacitance again, the C–V curve now resembles that of a regular MOS capacitance (see green line in figure 2(a)). While in low leakage, homogeneous luminescence in the whole area of the device can be detected from around $1.0\ \mathrm{A \cdot m^{-2}}$.

Figures 3(a) and 3(b) show the typical behavior of PECVD samples with different silicon excess. The C–V characteristics are quite similar to the expected from a MOS capacitance. Deep depletion can be observed in most samples and a displacement of the flat band voltage before and after the electrical stress can be seen for the lower silicon excesses. According to the hysteresis cycle, the amount of trapped charge and the oxide capacitance both increase along with silicon excess. The former is related to the increase of the density and size of the silicon nanoparticles[18]. From the latter we can infer an increase of the effective permittivity of the medium with the silicon excess[2], which is clear in the adimensional scale chosen for the y–axis of the C–V plots.

As with the LPCVD samples, a regular C–V curve is related to a low leakage current density (see figure 3(b)) and to homogeneous electroluminescence at around $1.0\ \mathrm{A \cdot m^{-2}}$. No luminescent dots are observed in PECVD samples.

The current density increases with silicon excess. However, samples with higher silicon excess are also more prone to breakdown. As a result, luminescence appears at lower voltages but the maximum achievable current before breakdown is also lower.

Ion Implanted samples show a slightly different C–V behavior (figure 4(a)). According to the width of the hysteresis cycle, the amount of trapped charge decreases as silicon excess is increased. There is also very little change in the C–V curves before and after the electrical stress. As with the PECVD samples, the relative permittivity of the medium increases with silicon excess, although there is little difference between the samples with 14% and 15% silicon excess. The samples with silicon excesses from 12% to 15% present homogeneous electroluminescence in the whole area from $1.0\ \mathrm{A \cdot m^{-2}}$.

The sample with 17% silicon excess presents an unstable C–V curve (figure 5) as well as high leakage current (figure 4(b), blue line). Similarly to what happened in the high leakage state in the LPCVD samples, no homogeneous electroluminescence is observed in this sample. Instead, only luminescent dots can be seen.

In the IV curves of the implanted samples it is also observed that the current density increases with silicon excess. The considerations about breakdown that we have discussed for the PECVD samples also apply here, although the differences are much less apparent, most likely due to the relatively small difference in silicon excess between samples.

4 Conclusions

We have shown the C-V and I-V behavior of MOS structures featuring silicon nanoparticles embedded in its dielectric matrix.

We have seen that there are two possible conduction regimes, one with low leakage and one with high leakage. The high leakage regime seems to be related to the formation of a finite number of conductive paths across the dielectric matrix. In this situation, almost all the current flows through those conductive paths. Therefore, the conduction through the active layer is not uniform and light is only observed in points corresponding to the places where the conduction takes place.

On the other hand, in the low leakage regime there are no such conductive paths and the current flows uniformly through the whole area of the layer. Accordingly, light emission also occurs uniformly in the whole area of the device.

The studied PECVD samples do not show a high leakage regime, whereas for implanted samples only the highest silicon excess shows such regime. The LPCVD sample presents both kinds of leakage: as-obtained devices show high leakage, which turns into low leakage after the application of an electrical stress. This behavior has been attributed to the annihilation of the preferential conductive paths[16].

It has also been shown that the low leakage regime is related to a regular MOS-like C-V behavior, whereas samples in high leakage regime show anomalous C-V, most likely related to the instability of the conductive paths.

A remarkable fact is that all the devices have a threshold current density of $1.0\ \mathrm{A} \cdot \mathrm{m}^{-2}$ before the emission starts, independently of the fabrication technique. This threshold is achieved at different electric fields depending on the silicon excess and the fabrication technique.

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