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Conservation of the optical properties of SRO after CMOS IC processing

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Abstract

The Silicon rich silicon oxide (SRO) is a CMOS compatible material that present light emission properties when annealed at high temperatures to produce the silicon segregation process. This material can be used to integrate optoelectronics circuits. However, during the CMOS fabrication process there are thermal processes that could alter the characteristics of this material. Moreover, in the same way thermal treatments needed for efficient light emission in the SRO could damage the electronic circuits. Then, special care has to be paid when SRO devices with optical functions and CMOS with electronic control circuits are integrated. In this paper, it is shown how a silicon sensor cover with a SRO layer and various electronic CMOS circuits were fabricated simultaneously. Details of how the SRO film was protected to avoid it to be damage, and how the SRO film was deposited and annealed in order to maintain the electronic circuitry working, are given. Experimental details of the optical properties and the electronic functionality are displayed. So, it is possible to integrate the SRO film and electronic functions in silicon IC successfully.

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Keywords: Silicon Rich Oxide; Optical properties; CMOS Optoelectronics integrated circuits.

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1. Introduction

There is not any doubt that current silicon technology has the biggest commercial impact in the world. Then, researchers have been looking for ways to incorporate functionalities not inherent to silicon. Visible light emission and sensing wavelengths smaller than 400 nm are examples of such properties [1]. Of course, regardless the proposed solutions, they have to be as much as possible compatible with the Si technology, in order to produce integrated circuits with working electronic devices together with those optical devices. Optoelectronic integrated circuits, for example, requires light sources, wave guides, detectors, etc., that today are faraway from being completely produced in silicon [2].

Nanometric materials have been extensively studied because they could be the answer to such expectations. For example, Silicon Rich Oxide (SRO), or off stoichiometric silicon oxide, has been studied due to its emission properties. As a matter of fact, it has been reported that it is possible to extend the sensing capabilities of silicon using this material, and also wave guides have been reported [3].

SRO can be obtained with different technologies. However, SRO obtained by low pressure chemical vapor deposition (LPCVD) offers various advantages: it can be obtained in a simple way and the silicon excess can be easily controlled using the ratio, Ro, of reactant gases:

$$Ro = P_{N2O} / P_{SiH4} \quad (1)$$

where P_{N2O} is the partial pressure of nitrous oxide and P_{SiH4} is the partial pressure of silane. Also, it provides one of the biggest emissions in the visible to near infrared range.

However, one disadvantage of using SRO is that it requires a high temperature treatment in order to produce the phase separation required to produce luminescence [4]. Regardless of the synthesis technique used, temperatures as high as 1250 °C are needed to get the emission ability. On this regard, SRO obtained by LPCVD requires only 1100 °C, which is another relative advantage. Extra care has to be paid during the thermal annealing, because the presence of oxygen could modify the material luminescent properties.

On the other hand, modern Si ICs (Integrated Circuits) technologies try to reduce as much as possible the thermal budget, then thermal treatments are kept as low and short as possible. Such is the case of the Metal Oxide Semiconductor (MOS) technique that is the most common ICs process. To expose the integrated circuit to thermal treatments different of the ICs processing could change the final functionality of the integrated circuit.

So, in order to integrate SRO devices, for example sensors, light emitters or waveguides, with Complementary Metal Oxide Semiconductor (CMOS) electronics, will require special processing steps to avoid damaging the CMOS electronics or the SRO devices.

In this paper, the SRO emissive properties are revised after being subjected to a CMOS fabrication process. Special process steps have been implemented in order to reduce the effect of the oxidation steps typical of CMOS process on the optical devices. At the same time the fabrication of the SRO devices have to be selected in such a way that the high temperature treatment does not disturb the CMOS process.

2. Experimental Issues

2.1. Initial experiment

SRO films with Ro = 30 and thickness of 550 nm were deposited on 3000 ohm.cm silicon wafers, named samples 1 and 2. The SRO films were deposited in a hot wall LPCVD system at 725 °C. After deposition, the film composition were analysed by Fourier Transform Infrared spectroscopy (FTIR) with a Bruker FTIR model Vector 22, with an interval from 400 to 4000 cm^{-1}. Thickness and refraction index were measured with a null elipsometer Gaertner L117 with a He-Ne laser in 632.8 nm and 70° of incidence. The photoluminescence (PL) characteristic were recorded with a spectrofluorometer Jobin Yvon Fluoromax-3, and excited with 270 nm. Then, the wafers were annealed at 1100 °C during 180 min in N_2 atmosphere. Null elipsometry and PL were again applied. Thereafter the wafers were covered with a 180 nm silicon nitride film, and subjected to main thermal annealing and implantations as in a standard CMOS process. The following heat treatments are the more outstanding: at 1200 °C, 4 hours and 45 minutes (the first 45 minutes were water oxidation; the remainder time was on nitrogen atmosphere), 7 hours and 30 minutes under wet oxidation at 950 °C, wet oxidation in oxygen and chlorine atmosphere for 1 hour and 25 minutes at 950 °C. After the CMOS process thermal simulation, the nitride was removed and the SRO parameters were measured again.

2.2. Integrated circuit and technology

CMOS-25 process from CNM (Centro Nacional de Microelectrónica, Barcelona, Spain) was used. This is a CMOS technology with a 2.5 microns minimum geometry, double well, two polysilicon levels and one metal.

Figs. 1 (a), (b) and (c) show different CMOS process profiles obtained by computational simulation. Fig. 1(a) shows the CMOS complementary transistor pair.

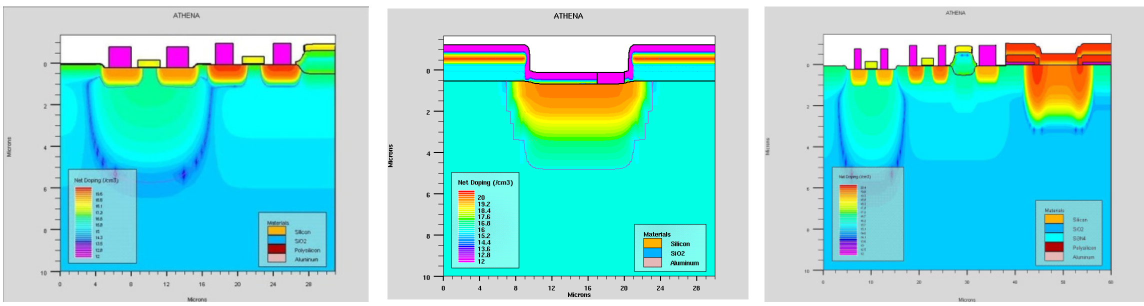
In order to demonstrate the integration of optoelectronics and CMOS circuitry feasibility, several electronic circuits were designed and special care was taken to have external input/output pads for all of them, also some of them were duplicated in an unconnected way. Table 1 resumes the circuits designed, also a discrete sensor with an area of 1.807×2.310mm^2 was fabricated in the same wafer. Fig. 2 is a microphotography of the fabricated IC.

Table 1. CMOS circuits included in the chip.

Circuit description	Quantity	Circuit description	Quantity
Current amplifier connected to a sensor	1	Current oscillator with output pads	1
Current amplifier with input/output pads	1	Output buffer with input/output pads	2
Operational amplifier with input/output pads	1	1323×1361um^2 Photodiode connected to an amplifier	1
Variable gain amplifier with input/output pads	1	276×281um^2 Photodiode with input/output pads	1
Current controlled oscillator with input/output pads	1	1807×2310um2 Photodiode with input/output pads (labeled “a” in Fig. 2)	1

2.3. The integrated sensor

SRO emits light in the approximate range of 600 to 900 nm when it is illuminated with UV light in the range of 200 to 350 nm approximately. This characteristic has been used to improve the light sensing in the UV range [1]. In a simple way UV detection is enhanced placing an SRO film on a silicon sensor. The SRO film works as a wavelength shifter. Fig. 3 shows a schematic of a discrete sensor, and Fig. 1(b) shows a profile of a sensor fabricated with the CMOS-25 technology obtained by computational simulation. The profile of a CMOS pair and the integrated sensor is presented in Fig. 1 (c), obtained also by computational simulation.



a) b) c)

Fig. 1. Transversal view of the technology obtained by computational simulation. (a) CMOS complementary transistor pair; (b) SRO sensor; and (c) CMOS pair and sensor.

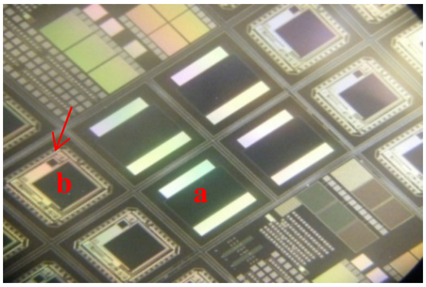


Fig. 2. Microphotography of the Si wafer with (a) discrete sensor with area 1.8 × 2.3 mm^2, (b) integrated circuit that include two sensors the big one is surrounded by the control electronics, and the small one can be seen at the upper right corner as indicated by the arrow..

As in the initial experiment, the SRO films were deposited in a hot wall Low Pressure Chemical Deposition system, 725 °C were used with Ro=20. The used reactant gases were SiH_4 and N_2O (Silane and nitrous oxide). Besides of the SRO deposition on the sensor, during this process also a SRO film was deposited on plain silicon wafers used as monitors, samples 45 and 46. The sensor integrated wafers and the monitors were annealed at 1100 °C in nitrogen atmosphere. The monitors were annealed during 3 hour, and the sensor wafer for 2 hour.

Subsequently, to protect the SRO of the oxidation needed in the CMOS process, a nitride layer was deposited and patterned on the active area only. The next step was to eliminate both the SRO around outside the nitride, and the protection of polysilicon. Then, the standard CMOS process continues. As a result, the SRO went into the thermal processes inherent to the CMOS technology, but it was covered with a protection as it is shown in Fig. 4.

After the fabrication of the CMOS circuit, some discrete diodes of 1.8× 2.3 mm^2 were cut off from the wafer and glued to a piece of printed circuit in order to enable its handling. PL measurements were done with a spectrofluorometer Jobin Yvon Fluoromax-3, exciting with 270 nm. The PL measurements were not so precise because the samples were small, and the excitation spot was bigger than the samples. That is, the excitation beam shines on some phenolic, cooper, and the Aluminum contact stripes at side of the sensors, see Fig. 2. So, to avoid abnormal emissions or reflections a black paper mask around the sensor was used. Also, different optical filters were tried in the input and output of the spectrometer to ensure that reflections and harmonics were eliminated.

3. Results and discussions

The need to have reliable light sources for optoelectronic devices requires of the simultaneous fabrication of various devices, for example waveguides and control electronics. Therefore, preservation of the optical properties of SRO after different thermal treatments and oxidations is absolutely needed. In this paper, the optical properties of the SRO were presented after the CMOS fabrication was achieved, and details of the electrical measurements will be presented in a future paper.

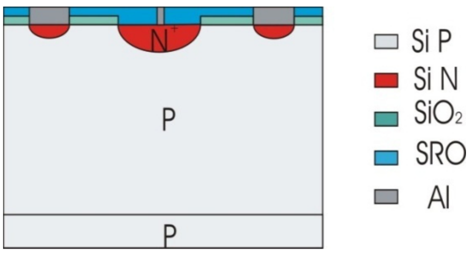


Fig. 3. Schematic of a discrete UV sensor out of scale.

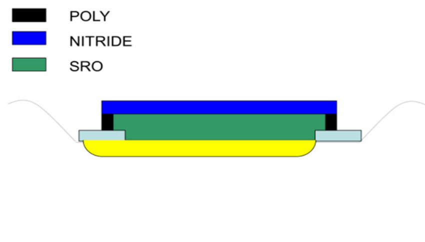


Fig. 4. Protection chamber around the SRO to avoid damages due to oxidation

3.1. Initial experiment

The initial experiment results of ellipsometry and PL are shown in Table 2 and Fig. 5 before and after the samples were subjected to the thermal CMOS treatments. These results agree with the standard ellipsometry, PL and FTIR measurements for this kind of samples with and without thermal annealing [5]. As can be seen, the CMOS thermal treatments do not alter the optical characteristics.

Table 2. Initial experiment ellipsometry results, the parameter after the samples were subjected to 1100 °C and the CMOS thermal treatments are presented under 1100 °C and MOS TT.

SAMPLE	Ro	Average thick nm	R index as deposit	R index 1100 °C	R index MOS TT
1	30	534.4	1.46	1.47	1.463
2	30	528.0	1.50	1.48	1.488

3.2. CMOS Process

In order to verify that the technology works as expected after circuit fabrication three tests are presented here. The first is the statistical analysis done for all the process on the circuit test chip. The results are presented in Table 3. The second is the I-V characteristic curves of the transistors, presented in Fig. 6, and finally the electric current results of one amplifier designed and fabricated in the chip.

Table 3. Parameter measured for the test chip fabricated in the same wafer with the MOS circuits and the sensor.

	Average	Stddev	Median	Number of Points
VTN30	0.955596	0.00907403	0.953824	23/24
BETAN30	57.9965	0.691504	58.1	23/24
VTP30	-1.13269	0.0120321	-1.13513	23/24
BETAP30	18.3617	0.195396	18.4	24/24
VTN30x3	0.871663	0.0239572	0.870545	24/24
BETAN30x3	1629.33	210.978	1643	24/24
VTP30x3	-1.09269	0.0242974	-1.09206	23/24
BETAP30x3	522.354	84.81	551.85	24/24
VTFN	14.8386	0.202578	14.8419	22/24
BETAFN	7.63902	0.227854	7.6225	23/24
VTFP	-16.5531	0.362385	-16.5117	22/24
BETAFP	1.75899	0.0446806	1.75167	23/24
IOFFN30	-11.3954	0.697852	-11.5422	24/24
IOFFP30	-11.6837	0.369733	-11.5763	24/24
IOFFFN	-11.7908	0.248431	-11.8097	23/24
IOFFFP	-11.7692	0.274815	-11.6874	22/24
IOFFN30x3	-11.7167	0.642093	-11.7645	21/24
IOFFP30x3	-11.6366	0.323757	-11.6073	21/24
LEFFN	1.0844	0.0952423	1.05332	23/24
LEFFP	1.03482	0.0879927	1.00621	23/24
RCMP+	9.675	1.91232	9.375	24/24
RCMN+	33.2771	8.82984	32.55	24/24
RCMP0	19663.1	3.18582	19663.5	22/24
RCMP1	4.52045	0.662006	4.5	22/24
R#P+	105.832	0.514667	105.997	24/24
R#N+	30.2261	0.432823	30.0382	24/24

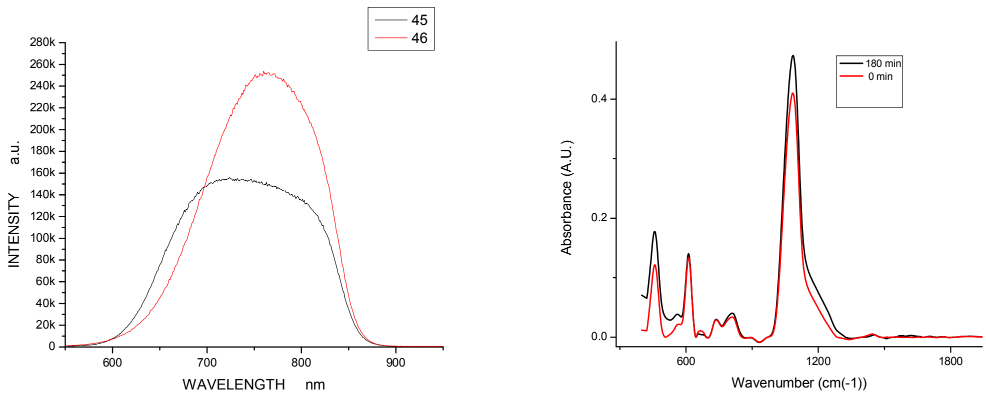
R#P0	9.8118e+12	3.65624e+13	-1.71693e+12	23/24
R#P1	21.2295	0.9593	20.9726	24/24
R#M1	0.0362714	0.00982931	0.0362734	21/24
R#NTUB	1328.7	19.7077	1326.71	24/24
R#P1AA	17.9229	0.865001	17.8529	24/24
DWP+	2.0031	0.0310057	2.009	22/24
DWN+	2.12256	0.0459266	2.12634	24/24
DWP0	332.728	915.885	-106.463	19/24
DWP1	2.30246	0.184472	2.24707	24/24
DWM1	2.71614	0.787687	2.65111	21/24
DWNTUB	8.67896	0.0938215	8.68692	24/24
DWP1AA	2.21853	0.228868	2.19939	24/24

The circuit schematic of the current amplifier is shown in Fig. 7(a). Due to its low input impedance and because it can drive large current variations, a Flipped-Voltage Follower (FVF) in current mode is used to sense the input current. The current mirror is used like a current amplifier, and its gain is obtained by the ratio W/L of the transistors M_1 and M_2 (1:10 in this case). The power supply is VDD = 9V and the generated voltage at the input node is 6.5V (node Iin between M1 and M3 and controlled by the bias voltage Vbp1); this voltage is used to keep the diode in reverse bias, as a photosensor. Bias current was set to 500 uA provided by Ms and Mc2. So, the input current will be amplified by a factor of 10 as is shown in Fig. 7(b), which presents experimental results of the fabricated current amplifier.

Clearly from Tables 3, and Fig. 6 and 7(b) the CMOS process works well after the joint fabrication of the sensor and the CMOS circuit.

3.3. Optical characteristics of SRO

Fig. 8(a) shows the PL of the monitors 45 and 46 obtained during the SRO deposition for the sensors, and Fig. 8(b) shows the PL emission spectrum of two sensors, after the MOS fabrication. The emission between 600 and 900 nm is characteristic of the SRO with Ro=20, as can be corroborated in Fig. 8(a), however an unusual emission was observed between 400 and 500 nm. Different excitation wavelengths were used to obtain the PL, in all of these measurements the characteristic emissions were always obtained. Fig. 9 shows a comparison between the monitors and the sensor emissions both excitation wavelengths were 270 nm. Clearly the emissive characteristic between 600 and 900 nm was preserved.



a) b)

Fig. 5. (a) Photoluminescence and (b) FTIR spectra of samples annealed at 1100 °C for 180 minutes before and after being subjected to the thermal treatments as CMOS.

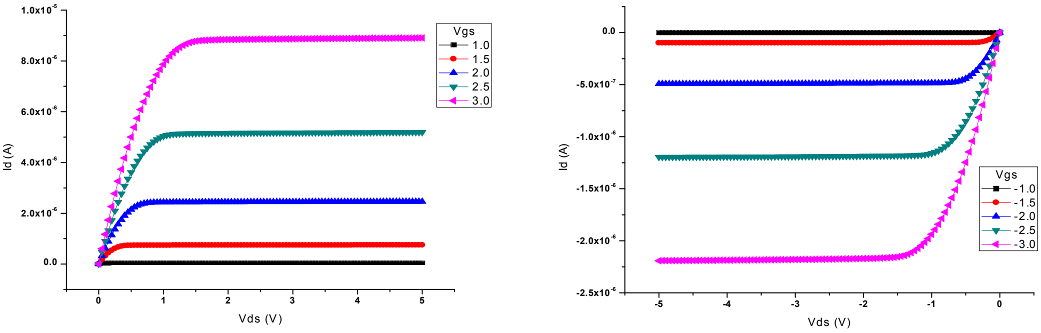


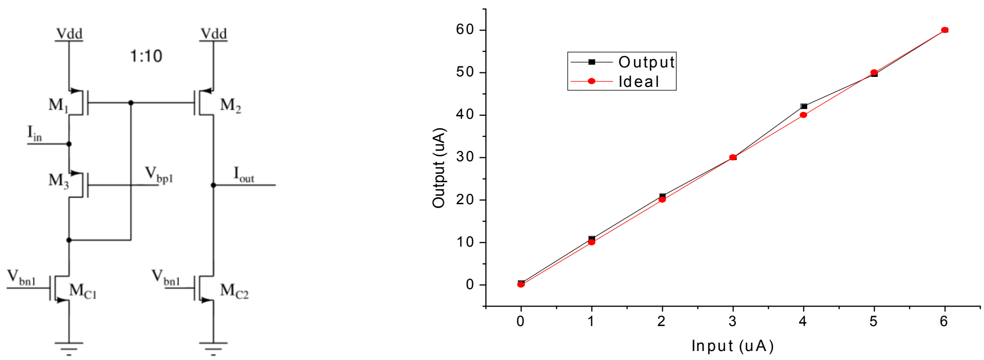
Fig.6. I-V characteristics of N and P Transistor fabricated together with the UV sensor.

In spite that different conditions and filters were used, the unexpected blue emission was always observed after the CMOS process. The PL of the sensor was measured with the sensor glued to a piece of printed board. Due to the small size of the sensor, cooper, Aluminum and phenolic material were exposed to the excitation, and then it could cause the blue emission. The measurement was repeated but masking all around the sensor with a non-emissive paper, however the Aluminum contacts were always exposed. The blue emission was higher when the printed board was exposed than when it was covered, and this fact suggests that the phenolic, the cooper or the Aluminum cause the spurious blue emission. Another possibility is that the protection nitride interacts with the SRO forming a surface layer producing the emission, however the fact the blue reduces when a mask shields the phenolic makes more probable the unauthentic radiation hypothesis.

Moreover from the result of the first experiment, it is clear that the characteristic emission of SRO is preserved after extra annealing steps due to CMOS processing, without blue emission, if the film is protected by a nitride layer.

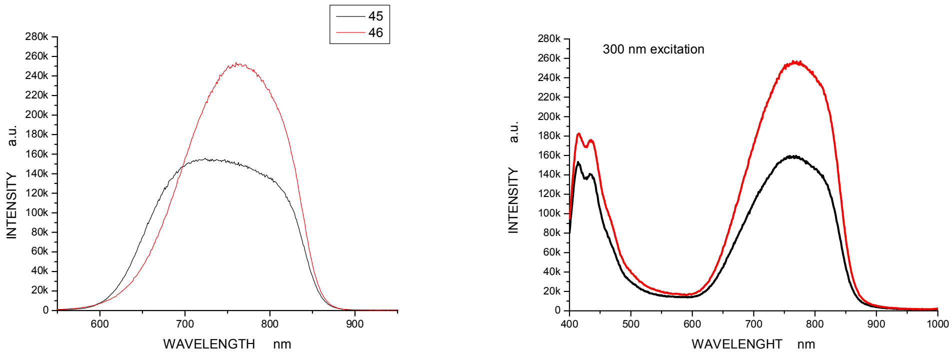
4. Conclusions

The emission of light in SRO subjected to extra thermal treatments was studied. Two experiments were done: in the first one, SRO films deposited on silicon wafers were cover with silicon nitride and then subjected to some thermal processes similar to that used in a CMOS process. In the second experiment a sensor with a SRO film on the top was integrated with CMOS electronic circuits. After the fabrication of the integrated circuit, the electronic circuits are working as designed, and details on these measurements will be presented in a future paper.



a) b)

Fig. 7. a) Designed amplifier with gain of 10X and integrated with CMOS technology and b) output as function of input current.



a) b)

Fig. 8. PL emission of (a) monitors with SRO20 after 1100 °C annealing for 3 hour in nitrogen and (b) two sensors mounted on a piece of printed board and cover with an opaque black paper. The Aluminum contacts are exposed to the excitation beam.

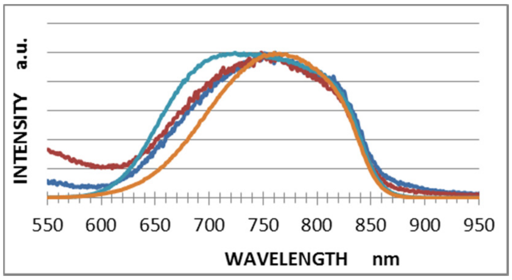


Fig. 9. PL emission of two monitors with SRO after 1100 °C for 3 hours (orange and pale blue), and emission of two diodes annealed at 1100 °C for 2 hours and then processed with the CMOS IC. The PL measured was on two discrete diodes.

In this paper, emission and other optical characteristics of both experiments were discussed. Comparison of the characteristics before and after being subjected to the extra thermal treatment was done. It is demonstrated that the SRO optical attributes are preserved if the SRO is covered with a silicon nitride film.

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